

## **AMENDMENTS TO THE SPECIFICATION**

The following amendments to the specification will replace all prior versions, and listings of claims in the application:

### **METHOD FOR TESTING CHIP CONFIGURATION SETTINGS**

#### **FIELD OF THE INVENTION**

The present invention relates to a method for testing a chip, more particularly to a method for testing chip configuration settings, essentially adding [[an]] a test process for the chip configuration settings into a BIOS program to perform the verification of configuration in the actual working environment as well as at the final stage before the operation is started.

#### **BACKGROUND**

Recently, the high development in information related industry and the trend in pursuit of speed, a variety of electronic and information products have been presented, and the ~~existed~~ existing products have also been reconditioned or renewed, for dazzling men. For the industry, it is unavoidable to perform various tests on samples with different specifications to verify whether the operation of the design is correct or not. Therefore, the quality control and test for several products [[may]] has become a significant issue [[of]] in [[the]] industry.

In the past, the development process, from design, through manufacture, and up to verification, for a new type of product performed by chip designers and manufactures is essentially shown as Fig. 1. ~~Firstly~~ First, the design for the chip is completed 101. The completed chip design is then tested under the simulation environment to check whether the chip design will ~~could~~ react properly on various commands ~~or not~~ 103. Only after having been confirmed, is engineering sample production for the chip 105 ~~[[is]]~~ allowed. After fabrication of the chip~~fabricated~~, for the purpose of performance testing ~~test~~, it is then necessary to prepare a corresponding main board for supporting the chip 107 ~~beforehand~~, to assemble a computer including the chip therein 109, ~~subsequently to~~ install the operating system of the computer and ~~[[a]]~~ software used for testing ~~[[test]]~~ 111, and finally to perform an on-board test and analysis for the chip 113. The chip may be put into market formally in the event of passing the test; otherwise, ~~[[the]]~~ a modification ~~[[for]]~~ to the chip design is necessary.

In general, most ~~[[of]]~~ errors in the logical circuit of the product design may be found and then corrected after the simulation verification process and a series of tests in the process 101, ~~as examples~~, have been completed. However, with the chip installed on the main board actually, there are possibly still some potential errors ~~occurred~~ that may occur at the regular operation, such as a wrong setting with respect to the configuration space, and the like, etc.

In the conventional art, the completed chip is first ~~of all~~ installed on the main board and the power on self test (POST) runs ~~is affected~~. Subsequently, the basic input/ output system (BIOS) is loaded and then ~~initialization for the chip is~~ initialized ~~effected~~. After the data and initial values of the chip setting in the chip configuration space have been read ~~[[out]]~~, the operating system is loaded for normal start.

During the aforementioned start process, the chip is initialized without verifying its configuration settings~~instead of the verification for the configuration setting of the chip, only the initialization for the chip is effected~~. At this moment, the operation of the chip may be different from the presetting target, ~~or yet further~~ resulting in abnormal operation, in the event ~~[[of]]~~ that ~~[[the]]~~ wrong configuration setting of the chip occurs.

Moreover, the initial values may be set under the assumption that the configuration space ~~setting~~ settings of the chip ~~[[is]]~~ are correct, ~~, such that it~~ It is hard to trace the source problem once the ~~operation of the~~ chip experiences problem due to the wrong configuration setting. As a result, repeated and complex precision testing tests, ~~even comparing one by one, are necessary,~~ is necessary for finding out where the key problem is. Therefore, ~~not only~~ a waste of time and labor, ~~[[an]]~~ increased manufacturing cost, ~~[[a]]~~ reduced product competition, and ~~but also~~ resistance for the development of new generation products may be encountered.

Thus, what is desired by users and intended to be solved by the present ~~inventor~~—invention for a long time is ~~that~~ proposing a novel solution, designing ~~[[an]]~~ a test method with high efficiency for not only testing the configuration setting of the chip, but also testing before the chip is placed on the main board for operating actually, in order to examine the actual operation of the chip, aiming at the disadvantages in the manufacture and test process for the aforementioned conventional chip. Actual experiences, in related research, development, and sale, in the information industry are the basis of the present ~~inventor~~ invention for the improvement. With several designs, studies, samples, and improvements, a method for testing chip configuration settings is thus invented for solving above problems.

### **SUMMARY OF THE INVENTION**

Accordingly, it is a primary object of the present invention to provide a method for testing chip configuration settings, essentially adding a configuration test process into a BIOS program to examine the actual effect of the configuration settings on the chip operation after the chip to be tested is installed on a main board.

It is a secondary object of the present invention to provide a method for testing chip configuration settings, wherein a test data table list is provided in the configuration test process for inputting to be tested.

It is another object of the present invention to provide a method for testing chip configuration settings, wherein an expected result data table list is provided in the configuration test process to be compared with an output result.

It is another object of the present invention to provide a method for testing chip configuration settings, wherein the configuration test process further comprises a step of recording a comparison result to be a reference served for correcting and developing the chip configuration.

The features, steps, and the effects to be achieved may further be understood and appreciated by reference to the following detailed description of the presently preferred embodiments together with the accompanying drawings, in which:

### **BRIEF DESCRIPTION OF DRAWINGS**

Fig. 1 is a flow chart of a conventional fabrication and test process for a chip;

Fig. 2 is a flow chart of a preferred embodiment of the present invention;

Fig. 3 is a flow chart of a configuration test process of the present invention;  
and

Fig. 4 is a diagrammatical view of a relationship between the respective modules in the test process of the present invention.

## DETAILED DESCRIPTION

First ~~Firstly~~, referring to Fig. 2, a flow chart of a fabrication process for a chip according to a preferred embodiment of the present invention is shown. Conventionally, for the chip industry, it ~~[[is]]~~ has always been assumed that, at the on board test testing provided after the chip ~~being~~ is fabricated completely, the configuration settings of the respective configuration registers in the configuration space of the chip are correct, the chip is then initialized for setting initial values, such that it becomes very difficult for testing the chip by other testing software after initialized. Even, the determining logics contradict such that the source of the error could not be concluded, due to base error produced by the initial values.

As illustrated in ~~the figure~~ Fig. 2, ~~[[an]]~~ a test method according to the present invention may comprise the steps as follows: first ~~firstly~~, starting power for the main board having the chip installed therein 201; after power is started, performing a power-on self-test ~~power-on self-test~~ (POST) process performed by the system 203; then, loading a basic input/output system (BIOS) program by the system 205, wherein the BIOS program may include a pre-written configuration test process; after the BIOS system is loaded, performing the configuration test process, testing each configuration setting for the chip 207; after tested, determining whether the configuration settings are correct or not depending on the tested result 209.

The configuration test process of the present invention could examine the actual reaction of the chip for analyzing it correctly, since the process is carried out just after the system ~~being~~ is started and prior to the chip is initialized, without the need of initial values provided for the chip by the system via initialization.

Next, referring to Fig. 3, a flow chart of the configuration test process according to the present invention is shown. The configuration test process of the present invention, the procedure steps ~~of which is~~ that are illustrated in the figure, may be written into the BIOS, and may be performed after the system ~~being~~ is started and prior to the chip ~~being~~ is initialized. ~~First~~ Firstly, inputting the prepared test data 301; enabling configuration registers corresponding to the configuration space of the chip depending on the need of the test data; and triggering the chip to perform the corresponding operation 303; afterward, obtaining the data produced by the chip operation 305; comparing the obtained data with the expected result in accordance with the design specification for the chip 307; then, writing the correct ~~correctness of the~~ comparison result and the difference ~~[[in-]]~~ between the result and the expected target into a record 309; creating a report with respect to the difference between the test result and the expected target, providing the industry with a basis for modifying the configuration space setting of the chip or ~~served~~ serve as ~~[[a]]~~ reference data for the development of a new generation product 311.

Finally, referring to Fig. 4, a diagrammatical view of a relationship between the respective modules in the test process according to the present invention is

shown. As illustrated in the figure, a test data table list 401 including at least one set of test data, and an expected result data table list 407 ought to be obtained from an ideal chip based on the operation of the test data, that may be ~~first-of-all~~ prepared by the industry in accordance with the design specifications for the chip. At least one set of output data 405 could be obtained from the chip based on the operation of respective test data, when the test data in the test data table list 401 is inputted into the configuration space 403. Then, the output data 405 as well as the corresponding expected result in the expected result data table list 407 are transmitted to a comparison module 421 to be compared with each other, and the result obtained from this comparison may be recorded in a comparison data table list 423. After that, a difference report 425, generated in accordance with said comparison result, may be provided as a basis for the modification of the chip configuration space as well as a reference for the development.

To sum up, it should be understood that the present invention is related to a method for testing a chip, particularly to a method for testing configuration settings of a chip, essentially provided to add a procedure for testing the configuration settings of the chip into the BIOS program, such that the verification for the configuration may be performed in the actual working environment as well as at the final stage before the operation is started. Thus, the correctness of the configuration settings could be found in the early phase, so as to speed the development and modification for the chip. Therefore, this application is filed in



accordance with the patent law duly, since the present invention is truly an invention with novelty, advancement or non-obviousness, and availability by the industry, thus naturally satisfying the requirements of patentability. Your favorable consideration will be appreciated.

The foregoing description is merely one embodiment of present invention and not considered as restrictive. All equivalent variations and modifications in process, method, feature, and spirit in accordance with the appended claims may be made without in any way from the scope of the invention.

#### **LIST OF REFERENCE SYMBOLS**

401	test data table list
403	chip configuration space
405	output data
407	expected result data table list
421	comparison module
423	comparison data table list
425	difference report